Amendments to the Specification:

Please amend the section "Brief Description of the Drawings" starting on page 6 as follows:

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIGURE 1 is a diagram of a CMP tool and wafer according to an embodiment of the instant invention.

FIGURE 2 is a plan view of a section of a CMP tool and wafer according to an embodiment of the instant invention.

FIGURE 3 is a plot of the signal intensity versus wafer position according to an embodiment of the instant invention.

FIGURE 4 is a plot of the signal intensity versus wafer position according to a further embodiment of the instant invention.

FIGUREs 5(a)and 5(b) are steps in a damascene process according to the prior art.

Common reference numerals are used throughout the figures to represent like or similar features. The figures are not drawn to scale and are merely provided for illustrative purposes.

Please amend the paragraph beginning on page 1, line 14 as follows:

--High speed integrated circuits use copper to form the metal lines that connect the various electronic devices that comprise the circuit. Copper lines are formed using a

damascene process that is illustrated in Figure 4-5(a) and Figure 4-5(b). As shown in Figure 4-5(a), a dielectric layer 310 is formed over a semiconductor 300. The semiconductor will contain electronic devices such as transistors that are omitted from the Figure for clarity. In a typical simply damascene process, a trench 315 is first formed in the dielectric layer 310. A barrier layer 320 is then formed over the surface of the dielectric layer and in the trench. Typical materials used to form the barrier layer include titanium nitride and other similar materials. Following the formation of the barrier layer 320, a copper layer 330 is formed. The copper layer is typically formed using a plating process and in addition to filling the trench 315, forms excess copper over the entire semiconductor surface. The excess copper is removed using chemical mechanical polishing (herein after CMP) resulting in the structure shown in Figure 4 5(b). The remaining copper line 315 is then used to interconnect various electronic devices that are formed in the semiconductor.